

Amendments to the Claims:

This listing of claims will replace all prior versions and listings of claims in the application:

Listing of Claims:

1. (currently amended) A power-gating technique for an integrated circuit device having a Sleep Mode of operation comprising:

providing an output stage directly coupled between a supply voltage source and a reference voltage source; and

driving a gate terminal of at least one element of said output stage to a level above that of said supply voltage source or below that of said reference voltage source in said Sleep Mode of operation.

2. (original) The power-gating technique of claim 1 wherein said output stage comprises series coupled P-channel and N-channel transistors coupled between said supply voltage source and said reference voltage source.

3. (original) The technique of claim 2 wherein said gate terminal of said N-channel transistor is driven below said reference voltage level while in said Sleep Mode of operation.

4. (original) The technique of claim 2 wherein said gate terminal of said P-channel transistor is driven above said supply voltage level while in said Sleep Mode of operation.

5. (currently amended) A circuit comprising:

an output stage comprising first and second series coupled transistors directly coupled between a supply voltage source and a reference voltage source, said output stage comprising an input terminal and an output terminal thereof;

a power-gating circuit coupled to a stage preceding said output stage for applying a voltage level to a gate terminal of said first transistor greater than that of said supply voltage source in response to a Sleep Mode of operation.

6. (original) The circuit of claim 5 wherein said output stage comprises a CMOS inverter and said first transistor comprises a P-channel transistor.

7. (original) The circuit of claim 5 wherein said voltage level applied to said gate terminal of said first transistor comprises substantially said supply voltage source level plus 0.3V.

8. (currently amended) A circuit comprising:

an output stage comprising first and second series coupled transistors directly coupled between a supply voltage source and a reference voltage source, said output stage comprising an input terminal and an output terminal thereof;

a power-gating circuit coupled to a stage preceding said output stage for applying a voltage level to a gate terminal of said second transistor lesser than that of said reference voltage source in response to a Sleep Mode of operation.

9. (original) The circuit of claim 8 wherein said output stage comprises a CMOS inverter and said second transistor comprises a N-channel transistor.

10. (original) The circuit of claim 8 wherein said voltage level applied to said gate terminal of said second transistor comprises substantially said reference voltage source level minus 0.3V.

11. (currently amended) An integrated circuit device including a power-gated write data driver circuit for a memory array, said driver circuit comprising:

at least a first stage coupled between a supply voltage source and a power-gated reference voltage line;

an output stage directly coupled between said supply voltage source and a reference voltage source, an input to said output stage being coupled to an output of said at least said first stage; and

a power-gating circuit coupled to a stage preceding said output stage for driving said input to a level lower than that of said reference voltage source level in response to a Sleep Mode of operation.

12. (original) The integrated circuit device of claim 11 wherein said output stage comprises a CMOS inverter comprising at least one series coupled P-channel transistor and at least one N-channel transistor.

13. (original) The integrated circuit device of claim 12 wherein a gate terminal of said at least one N-channel transistor is driven to establish a negative V_{GS} in response to said Sleep Mode of operation.

14. (currently amended) An integrated circuit device including a power-gated write data driver circuit for a memory array, said driver circuit comprising:

at least a first stage coupled between a reference voltage source and a power-gated supply voltage line;

an output stage directly coupled between a supply voltage source and said reference voltage source, an input to said output stage being coupled to an output of said at least said first stage; and

a power-gating circuit coupled to said input of said output stage for driving said input to a level higher than that of said supply voltage source level in response to a Sleep Mode of operation.

15. (original) The integrated circuit device of claim 14 wherein said output stage comprises a CMOS inverter comprising at least one series coupled P-channel transistor and at least one N-channel transistor.

16. (cancelled)
17. (new) A power-gating technique for an integrated circuit device having a Sleep Mode of operation comprising:
 - providing an output stage directly coupled between a supply voltage source and a reference voltage source; and
 - driving a common gate terminal of said output stage to a level above that of said supply voltage source in said Sleep Mode of operation.
18. (new) The power-gating technique of claim 17 wherein said output stage comprises series coupled P-channel and N-channel transistors coupled between said supply voltage source and said reference voltage source, and to the common gate terminal.
19. (new) A power-gating technique for an integrated circuit device having a Sleep Mode of operation comprising:
 - providing an output stage directly coupled between a supply voltage source and a reference voltage source; and
 - driving a common gate terminal of said output stage to a level below that of said reference voltage source in said Sleep Mode of operation.
20. (new) The power-gating technique of claim 19 wherein said output stage comprises series coupled P-channel and N-channel transistors coupled between said supply voltage source and said reference voltage source, and to the common gate terminal.